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09/880,404	06/12/2001	Akila Sadhasivan	42390P10595	7126

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EXAMINER
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ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *12 June 2001* .

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-24* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-24* is/are rejected.

7) ☒ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

     If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All b)☐ Some * c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____ .

         3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

     a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: ____ .

DETAILED ACTION

1.   The present Office Action is a Non-Final Action taken in response to examination of

Claims 1-24, presented in the application. Applicant is reminded that each individual associated

with the filing and prosecution of a patent application has a duty of candor and good faith in

dealing with the Office, which includes a duty to disclose to the Office all information known to

that individual to be material to patentability as defined in 37 CFR 1.56.

Drawings

2.   The drawings are objected to because of the following informality: a typographical error.

A proposed drawing correction or corrected drawings are required in reply to the Office action to

avoid abandonment of the application. The objection to the drawings will not be held in

abeyance.

In Figure 3, element 42 should be changed from "READ DATE" to "READ DATA".

3.   Applicant's cooperation is requested in correcting any errors of which applicant may

become aware in the specification, the drawings or the claims.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the
invention by the applicant for patent, except that an international application filed under the treaty defined in

section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5.   Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (United States Patent 6,377,486).

With respect to Claims 1-2, and 6-7, Lee teaches a method of performing multiple operations on a flash memory device (EEPROM) comprising: dividing the memory device into k non-overlapping partitions (e.g., Figure 3; Column 5, line 35 to Column 6, line 61), wherein k is an integer greater than or equal than two; performing code operations from m code partitions (e.g., boot blocks) out of k total partitions; performing data operations from n data partitions (e.g., normal blocks) out of k total partitions through low level functions accessed from the code partitions wherein n is an integer greater than or equal to one.

Regarding Claim 3, Claim 1 is addressed above. Lee also teaches that the boot block and the normal block comprise the total k partitions in the nonvolatile memory array (e.g., Figure 3).

Regarding Claim 4, Claim 3 is addressed above. Lee also teaches that each of the m code partitions is equal in size to each of the data partitions (e.g., 8 megabits per block).

Regarding Claim 5, Claim 3 is addressed above. Lee also teaches that once a particular architecture is selected, the partitions are fixed in memory space (e.g., Columns 3-4).

7.   Claims 8-16 and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Brown et al (United States Patent 6,201,739).

With respect to Claim 8, Brown et al teach an apparatus comprising a means for partitioning a memory device (e.g., code and data partitions) to enable multiple operations to be performed on a memory device at the same time; and a means for tracking operations performed on the device to restore interrupted tasks (e.g., Column 8).

Regarding Claims 9 and 10, Brown et al also teach a means for saving a preempted state before entering an interrupt routine and restoring a preempted task following an interrupt routine (e.g. resume capability; Column 8).

With respect to Claims 11-14, Brown et al teach a flash memory array comprising a plurality of partitions, wherein code is programmed into the array (i.e., code and data; e.g., Figure 10), along with a status mode, a read, a write mode, and an erase mode (e.g., Column 7, line 19 to Column 9, line 45).

With respect to Claim 15, Brown et al teach handling a preemption within a flash memory device comprising: saving the preempted state (e.g., Column 8); reading the current state from the flash memory device (e.g., Figures 11-13); determining whether the flash memory device is busy (e.g., Figure 12); setting the memory device to a preempting state (e.g., Figures 11-14); issuing a preempting command (e.g., Figures 11-14); executing the preempting command and restoring the preempted state (e.g., Figures 11-14).

Regarding Claim 16, Claim 15 is addressed above. Brown et al further teach suspending a preempted task if the flash memory device is busy prior to issuing a preempting command (e.g., Figure 12).

With respect to Claims 19, Brown et al teach a memory device with k partitions (e.g., code and data partitions, Figure 10), wherein k is an integer greater than or equal to two; low

level functions to access the memory device (e.g., Figure 9); and a flag to indicate when a

suspend operation has occurred (e.g., the signal referred to in Figure 11).

Regarding Claims 20-21, Claim 19 is addressed above. Brown et al teach a flash

memory device comprising at least one code partition and at least one data partition (e.g.,

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

9.   Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al

(United States Patent 6,201,739) in view of See et al (United States Patent 6,189,070).

Regarding Claims 17-18, Claim 16 is addressed above. However, Brown et al does not

specifically mention disabling interrupts prior to issuing the preempting command, wherein the

preempting command is a write, an erase, or a copy. Brown also does not specifically mention

further enabling interrupts after the preempting command. See et al, however, teach disabling

interrupts prior to issuing a preempting command and enabling the interrupts after completion

(e.g., Figure 4; Columns 5-6). Thus, it would have been obvious to one of ordinary skill in the

art at the time the invention was made to combine the teachings of See et al with Brown et al

because it would provide for a flash memory device capable of implementing certain commands

without disruption and would further provide for the retrieval of valid data upon a later access.

9.   Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over See et al

(United States Patent 6,189,070).

Regarding Claims 22-24, See et al teach a flash memory block performing a preempting

programming (i.e. writing). See et al teaches placing the current state in read mode, placing the

current state in status mode, disabling interrupts, performing a write setup, unlocking a memory

block, writing to memory, and enabling interrupts (e.g., Figure 4). Although, See et al does not

specify a copy instruction and thereby does not specifically mention issuing the read command to

access data to be copied and retrieving data to be copied, these features and steps are known and

are common in the implementation of a copy instruction. Thus, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to specify these steps as they

are common steps and features in a copy instruction and the inclusion of a copy instruction in the

system of See et al would allow for a direct means of duplicating a data element.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kathy Takeguchi whose telephone number is (703) 305-8115.

The examiner can normally be reached on Monday - Friday, 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mr. Do H. Yoo can be reached on (703) 308-4908. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 746-7239 for regular

communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 305-3900.

KT
Kathy Takeguchi
Art Unit 2187
March 10, 2003

DO HYUN YOO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100